

Ultra-Low Power Extreme Environment Capable Avionics System-on-a-Chip

Completed Technology Project (2012 - 2013)



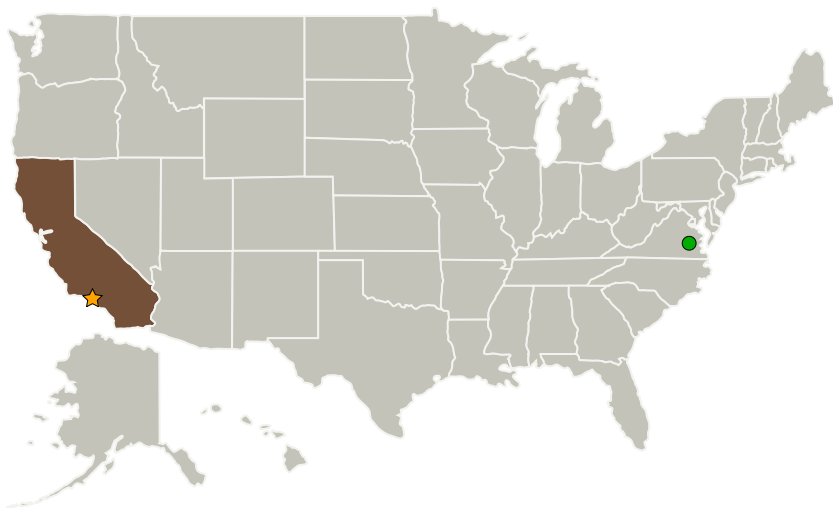
Project Introduction

Develop ultra-low-power, wide-temperature (-150°C to $+250^{\circ}\text{C}$), digital System-on-a-Chip (SOC) ASIC technology in a high resolution, inherently rad-hard IBM Silicon-on-Insulator (SOI) CMOS process to enable next-generation flight electronics. Demonstrate main flight-system electronics (flight processor, high- and low-speed instrument interfaces) in a chip containing a Cortex-M0 microprocessor that has been synthesized using a custom wide-temperature digital logic library developed in the same high resolution IBM SOI CMOS process.

Anticipated Benefits

The new SoC ASIC has a very good chance of setting NASA on a path to produce low-cost, ARM-based, SoC ASICs for avionics applications.

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★ Jet Propulsion Laboratory (JPL)	Lead Organization	NASA Center	Pasadena, California
● Langley Research Center (LaRC)	Supporting Organization	NASA Center	Hampton, Virginia



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Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Jet Propulsion Laboratory (JPL)

Responsible Program:

Center Innovation Fund: JPL CIF

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Primary U.S. Work Locations

California

Project Management

Program Director:

Michael R Lapointe

Program Manager:

Fred Y Hadaegh

Project Manager:

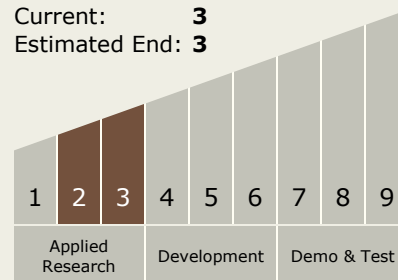
Jonas Zmuidzinias

Principal Investigator:

Ryan A Stern

Technology Maturity (TRL)

Start: 2
Current: 3
Estimated End: 3



Technology Areas

Primary:

- TX02 Flight Computing and Avionics
 - └ TX02.1 Avionics Component Technologies
 - └ TX02.1.6 Radiation Hardened ASIC Technologies